(Translation)

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Response Due: 2003.05.28

Patent Office

NOTIFICATION FOR FILING OPINION

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Patent Application No.: 10-2001-0035711

Title of the Invention: SEMICONDUCTOR INTEGRATED CIRCUIT AND SEMICONDUCTOR DEVICE SYSTEM

After examining the present application, the Examiner has confirmed that the present application contains the following reasons for rejection, and this notification is mailed under Section 63 of the Patent Law. A written opinion and/or an Amendment, if any, must be submitted by the above-noted due date. (The due date can be extended in units of one month upon request, and no notification will be sent about whether or not the extension of the due date is permitted.)

REASONS

The invention recited in the claims of the present application is unpatentable under Section 29 (2) of the Patent Law as being readily made by those skilled in the art on the basis of the references set forth below.

REMARKS

The present invention relates to a semiconductor integrated circuit mainly comprised of a reference potential conversion circuit and an input circuit. The present invention is similar to the technical means (idea) of Korean Patent Laid-Open Application No. 2000-004505 (2000.1.25), wherein a reference voltage converter converts a reference voltage generated by a reference voltage generator into a power supply voltage required for an internal circuit operation, and the voltage obtained by this conversion is compared and output. The